

APPLICATION

FOR

UNITED STATES LETTERS PATENT

**TITLE: PACKAGING MICROELECTROMECHANICAL
STRUCTURES**

**INVENTORS: QING MA, VALLURI RAO, LI-PENG WANG,
JOHN HECK and QUAN TRAN**

Express Mail No. EV 337 932 428 US

Date: August 19, 2003

PACKAGING MICROELECTROMECHANICAL STRUCTURES

Background

This invention relates generally to microelectro-mechanical systems (MEMS) and particularly to techniques for packaging MEMS.

5 In some cases, MEMS components such as varactors, switches and resonators need to be packaged in a hermetic environment. For example, particularly with radio frequency MEMS components, there may be a need for hermetic packaging. Such packaging protects the MEMS components
10 from the outside environment.

Conventionally, two approaches have been utilized for hermetic packaging of MEMS components. Ceramic packages with cavities that may be sealed are used in the defense industry. This approach, while reliable, may be cost
15 prohibitive for many commercial applications.

A second approach is to use a glass frit to bond a wafer containing the MEMS components to a cover. However, this technique requires high temperature bonding that may not be suitable for all components utilized in some MEMS
20 applications. In some cases, the glass frit occupies a large area that increases the size of the resulting product and therefore increases its costs. In some cases, the glass frit bonding technology uses wire bonds for

electrical connections that may not be adequate in some applications, such as high frequency applications.

Thus, there is a need for better ways to package MEMS components.

5 Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of one embodiment of the present invention;

Figure 2 is an enlarged cross-sectional view of the embodiment shown in Figure 1 early in the manufacturing
10 process in accordance with one embodiment of the present invention;

Figure 3 is an enlarged cross-sectional view of the embodiment of Figure 1 early in the manufacturing process according to one embodiment;

15 Figure 4 is an enlarged cross-sectional view at a subsequent stage of the manufacturing process according to one embodiment;

Figure 5 is an enlarged cross-sectional view at a subsequent stage of the manufacturing process according to
20 one embodiment;

Figure 6 is an enlarged cross-sectional view at a subsequent stage of the manufacturing process according to one embodiment;

25 Figure 7 is an enlarged cross-sectional view at a subsequent stage of the manufacturing process according to one embodiment;

Figure 8 is an enlarged cross-sectional view of another embodiment of the present invention;

Figure 9 is an enlarged cross-sectional view at an early stage of manufacturing the embodiment shown in Figure 9 in accordance with one embodiment of the present invention;

Figure 10 is an enlarged cross-sectional view at an early stage of manufacture of the embodiment shown in Figure 9 in accordance with one embodiment of the present invention;

Figure 11 is an enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 12 is an enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention; and

Figure 13 is an enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a packaged microelectro-mechanical system (MEMS) 10 may include an upper semiconductor structure 14 and a lower semiconductor structure 12. The structures 12 and 14 are electrically and mechanically coupled through bond pads 16a and 16b and

a vertical wall 18 that extend completely around the periphery of the system 10.

Within the system 10 is a MEMS device 34 that may be contained within a hermetic cavity 44. Also contained
5 within the cavity 44 in one embodiment is a film bulk acoustic resonator (FBAR) 32 that includes a membrane positioned over an open area 38. Similarly, a transmission line 30 may be fabricated over another open area 38. An electrical connection from the exterior of the system 10
10 can be made by way of a surface mount connection 28, in one embodiment through a via 40 to a bond pad 16c that electrically contacts the transmission line 30. A transmission line 30 may electrically couple the film bulk acoustic resonator 32 or the MEMS switch 34 to a connection
15 28 for electrical connection to the exterior of the system 10.

The lower semiconductor structure 12 may include a layer 20 that closes the open areas 38. The bond pad 16a may be positioned on a layer 26 that, in one embodiment of
20 the present invention, may be an insulator. In this way, electrical communication may be had between the transmission lines 30, the switch 34, the resonator 32, and other devices within the cavity 44 in the wall 18, through surface mount connections 28 in one embodiment of the
25 present invention. At the same time, the various MEMS components such as a switch 34, the transmission line 30,

and the resonator 32 may be electrically connected as desired. Some components, such as the resonator 32 and the transmission line 30, may be positioned over voids or open areas 38 in accordance with some embodiments of the present invention.

Referring to Figure 2, the lower semiconductor structure 12 may be formed of a semiconductor substrate 24 that may be part of a wafer in one embodiment. An insulator layer 26 may be formed on the substrate 24. A bonding pad 16a may be formed on the insulator layer 26. Also defined over the insulator layer 26 is the MEMS switch 34 and the transmission lines 30. The transmission lines 30 may each be coupled to a bonding pad 16c. The film bulk acoustic resonator 32 may be formed directly over the substrate 24 in one embodiment of the present invention.

Referring next to Figure 3, a cavity 42 may be formed in the upper semiconductor structure 14 that may be part of a wafer in one embodiment. The structure 14 may have a bonding pad 16b coupled to the vertical wall 18 that encircles the entire structure 14. The wall 18 may be made of solder or gold metal, in one embodiment.

The structures 12 and 14, shown in Figures 2 and 3, are then brought together, as shown in Figure 4, and, in some cases, pressure may be applied. At moderate temperatures, the wall 18 seals to the bonding pad 16a sealingly forming a cavity 44. Depending on the

environment in which the cavity 44 is formed, an appropriate atmosphere may be defined inside the cavity 44. Because surface mount techniques are utilized in some embodiments, the structure shown in Figure 4 may be formed
5 at temperatures of less than 300°C. In some cases, pressure may be applied to the structures 12 and 14 to ensure complete bonding.

Next, in some embodiments, the semiconductor substrate 24 may be thinned as shown in Figure 5. Grinding or
10 etching may be utilized in some embodiments and then a hard mask 22 may be formed. By thinning the wafer at this point, the bulk silicon etching time, in a later step, may be reduced also saving real estate if anisotropic etching is used in that subsequent step.

15 Turning next to Figure 6, openings may be formed through the hard mask 22 and through the remainder of the semiconductor substrate 24 to form the open areas 38 and to form additional open areas 46. In some embodiments, a silicon bulk etch such as deep reactive ion etching (DRIE)
20 or wet anisotropic etch may be utilized.

Referring to Figure 7, the layer 20 may be formed over an open area 38. The layer 20 may be a plastic or other organic film such as a polyimide film. In one embodiment, a KAPTON® foil from E.I. duPont de Nemours Co. (Wilmington,
25 Delaware) may be utilized. The layer 20 may be secured, for example, using glue, such as epoxy, to the hard mask

22. In addition, an enlarged opening 48 may be formed through the layer 20 to connect to the opening 46.

In some embodiments, a dielectric layer 50 may be formed on the sidewalls of the openings 46 and 48. The
5 dielectric layer 50 may be useful in some embodiments to avoid reaction, for isolation, and to reduce parasitic capacitance. In some embodiments dielectric deposition may be achieved by low temperature vapor coating followed by a directional etch to clear the pads 16c.

10 Referring again to Figure 1, solder may be screen printed or otherwise applied in the aperture formed by the openings 46 and 48 to form surface mount connections 28 and vias 40. As a result, electrical connection is available from the exterior of the system 10 through the connection
15 28 to the via 40 to the bond pad 16c and then on to the transmission line 30, in one embodiment of the present invention. The transmission line 30 may couple MEMS components such as the switch 34 and the FBAR 32. The FBAR 32 is now positioned as a membrane over an opening 38.
20 Similarly, the transmission line 30 may be positioned over an opening 38, which may provide electrical isolation from the underlying substrate 24 to reduce the coupling of noise, for example.

In some embodiments, a variety of radio frequency MEMS
25 components may be formed inside the same system 10. A switch 34 is an example of a MEMS device with a

mechanically moving part that needs a solid substrate. The FBAR is an example of a membrane device located over an area where the silicon needs to be etched away. The devices 32 and 34 may be provided in a common cavity 44.

5 It is also possible that multiple devices are located in the cavity 44 or that multiple devices are maintained in separate cavities.

By using a surface mountable wall 18 and moderate temperatures, the entire structure may be formed without
10 interfering with delicate MEMS systems. Since the entire structure may be formed on a wafer at the wafer level, it is not necessary to deal with individual silicon dice in some embodiments. At the same time, electrical inputs and outputs may be readily realized using interconnects that
15 run through the semiconductor structure 12 in one embodiment.

Semiconductor material underneath the transmission lines 30 may be etched away to reduce substrate losses, and semiconductor material under the resonator 32 may be
20 removed to form a membrane. Even if the resulting lower structure 12 is weakened, the overall system 10 may have sufficient strength due to the operation of the upper semiconductor structure 14. In some embodiments, surface mounting techniques may be utilized which require lower
25 temperatures and which provide better radio frequency connections than wire bond connections.

Referring to Figure 8, a MEMS system 10a includes a lower semiconductor structure 12a and an upper semiconductor structure 14a. In one embodiment, the upper structure 14a may be formed of glass to reduce substrate related parasitic capacitance and losses due to induced currents. Surface mount connections may be formed through the structure 14a instead of the structure 12a in some embodiments. Otherwise, the structure 12a is the same as the structure 12 shown in Figure 1.

Electrical connections may be made through the structure 14a by a surface mount connection including an upper portion 64, an intermediate portion 62, and a lower portion 66. A dielectric coating 60 may be applied between the intermediate portion 62 and the structure 14a in some embodiments. The lower portion 66 may be surface mounted to a bonding pad 16c on the structure 12a. Surface mount connections may be made to external components using the upper portion 64, which may be a solder bump.

The structure 12a, shown in Figure 9, may include bonding pads 16c. The bonding pads 16c, sometimes referred to as a wettable layer, communicate with the transmission lines 30. The fabrication of the structure 12a is otherwise the same as the fabrication of structure 12 described previously.

The upper structure 14a may be a glass or ceramic wafer with wafer vias and solder bumps as shown in Figure

10. The via holes may be formed by DRIE, powder blasting, or laser drilling, to mention a few examples. The dielectric layer 60 may be a coating that acts as a plating seed layer. The portions 62, 64, and 66 are plated in one
5 embodiment.

The upper structure 14a and the lower structure 12a may be bonded to one another in a desired environment (such as nitrogen or vacuum) at moderate temperatures, for example, less than 300°C as shown in Figure 11. Adequate
10 pressure may be applied for complete bonding. Surface mount techniques may be utilized to cause the lower portions 66 to surface mount to the bonding pads 16c.

The lower semiconductor structure 12a may then be processed as shown in Figure 12, as described previously in
15 connection with Figure 5.

Similarly, as shown in Figure 13, the open areas 38 and 36 may be formed, as described previously in connection with Figure 7. The open areas 46 are unnecessary. The layer 20 may then be applied as shown in Figure 1 to define
20 the open areas 38, as described previously in connection with Figure 8.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and
25 variations therefrom. It is intended that the appended